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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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DALLAS, TX 75265

EXAMINER

STARK, JARRETT J

ART UNIT	PAPER NUMBER
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2823

NOTIFICATION DATE	DELIVERY MODE
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12/12/2008

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/810,905	Applicant(s) BU ET AL.	
	Examiner JARRETT J. STARK	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 July 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 11-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10, 19 and 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 2/26/2008 directed to the cited prior art references individually have been fully considered but they are not persuasive.

Applicant's arguments with respect to the newly amended claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad (US 6,037,639) in view of Chen et al. (2005/0136583 A1).

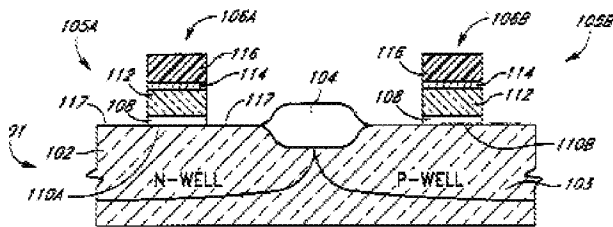


Fig. 1

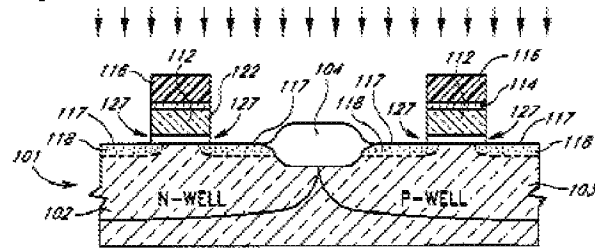


Fig. 2

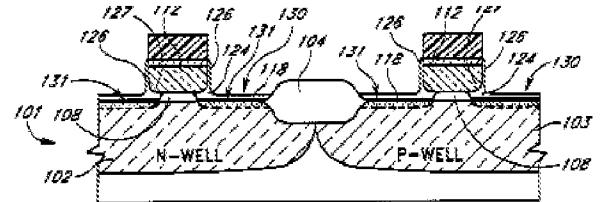


Fig. 3

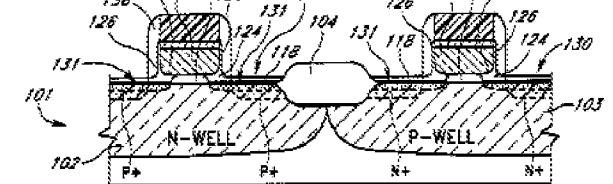


Fig. 4

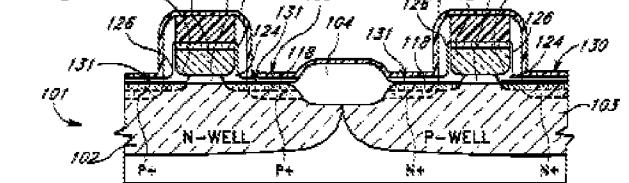


Fig. 5

Regarding claim 1, Ahmad discloses a method for fabricating a CMOS transistor structure, comprising the steps of:

providing a semiconductor substrate having a P-type dopant region to support an N-channel transistor of the CMOS transistor structure and an N-type dopant region to support a P-channel transistor of the CMOS transistor structure, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure (Fig. 1)

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack (Ahmad, Fig. 2);

forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (Ahmad, Fig. 3 –[126]);

forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (Ahmad, Fig. 3, Col. 1 line 66 to Col. 2 line 11 and/or Col. 2 lines 44-61);

forming at least one sidewall layer coupled to the layer of insulating material (Ahmad, Fig. 4 –[136]);

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks (Ahmad, Fig. 4);

forming a capping layer of contiguous silicon nitride over the semiconductor substrate (Ahmad, Fig. 5 - [138]).

Annealing is implicitly understood step that is required in order activate the dopants.

Ahmad is however silent upon explicitly annealing, after the formation of the capping layer and with the capping layer in place, then removing all of the capping layer after the annealing.

This sequence of steps was however conventionally known to one of ordinary skill in the art at the time of the invention.

At the time of the invention it was known in that the induced strain/stress in the channel region of a CMOS device can be modified by performing the annealing step with the capping layer in place. This known processing sequence when forming a CMOS device is disclosed by Chen et al. Chen discloses the sequence of steps comprising:

forming a capping layer of contiguous silicon nitride over the semiconductor substrate (Chen, Fig. 3 - [24]);

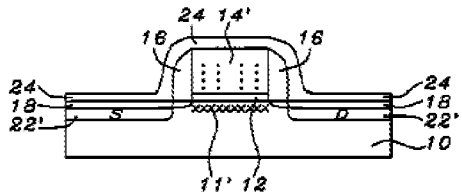


FIG. 3

annealing, after the formation of the capping layer and with the capping layer in place, the extension regions and the source and drain regions (Chen, Fig. 4 - [27] paragraph [0051]); and

and then teaches that the capping layer is capable of being removed after the annealing (Chen, Fig. 5 - [27] paragraph [0059]);

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Ahmad and Chen to enable the CMOS production step of Chen to be performed according to the teachings of Chen because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed CMOS production step of Chen and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

NOTE: Chen et al. discloses all of the claimed limitations except for the step of implanting a interfacial layer of nitrogen. Additionally, it would be obvious to one of ordinary skill in the art at the time of the invention, in view of Ahmad, to perform an additional step of forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions, merely to achieve

Art Unit: 2823

the benefits associated to the silicide formation as disclosed by Wieczorek.

Claims 2–10 and 19 -20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad in view of Chen et al. in further view of Wieczorek et al (US 2004/0061228 A1).

Regarding claims 2-3, Ahmad in view of Chen disclose the method of claim 1. Ahmad is however silent upon the desired dopant concentration for the source and drain regions. It would however be obvious to one of ordinary skill in the art to be capable of selecting the proper doping concentration from conventionally known ranges to meet the desired design/operating parameters of the device being manufactured. For a supporting example of one of ordinary skill in the art disclosing the claimed convention doping concentration range see Wieczorek, paragraph [0034]. Wieczorek disclosed wherein the extension, source, and drain regions for the PMOS transistors have a dopant concentration in the range of about $1-2 \times 10^{20}$ atoms/cm³.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the dopant concentration through routine experimentation and optimization to obtain optimal or desired device performance because the dopant concentration is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the

Art Unit: 2823

optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller*, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation." Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 4, Ahmad in view of Chen disclose the method of claim 1 wherein said interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent (Ahmad, Col. 4 lines 8-15).

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the nitrogen concentration through routine experimentation and optimization to obtain optimal or desired device performance because the nitrogen concentration is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to

Art Unit: 2823

discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller*, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation." Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 5, Ahmad in view of Chen disclose the method of claim 1 wherein the insulting layer is selected from the group comprising silicon nitride and silicon oxide (Ahmad, Fig. 3 –[126], Col. 1 line 66 to Col. 2 lin 11 and/or Col. 2 lines 44-61);

Regarding claim 6, Ahmad in view of Chen disclose the method of claim 1 wherein the step of forming an interfacial layer of nitrogen is performed using one of the methods selected from the group comprising an NH₃ thermal

Art Unit: 2823

annealing, an NH₃ or N₂ plasma treatment, or an N implantation (Ahmad, Fig. 3 –[126], Col. 1 line 66 to Col. 2 line 11 and/or Col. 2 lines 44-61);

Regarding claim 7, Ahmad in view of Chen disclose the method of claim 1 wherein the capping layer has a thickness in the range of 200-1000 angstroms (Chen, paragraph [0048], Ahmad discloses the capping layer however is silent upon the thickness).

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the thickness through routine experimentation and optimization to obtain optimal or desired device performance because the thickness is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

Regarding claim 8, Ahmad in view of Chen disclose the method of claim 1 wherein the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds (Chen, paragraph [0051] RTA will be below 10 seconds).

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the temperature through routine experimentation and optimization to obtain optimal

Art Unit: 2823

or desired device performance because the temperature is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

Regarding claim 9, Ahmad in view of Chen disclose the method of claim 1 wherein the step of forming at least one sidewall layer includes the use of a BTBAS precursor (Chen, paragraph [0046]).

Regarding claim 10, Ahmad discloses a method for fabricating a CMOS transistor structure, comprising the steps of:

- providing a semiconductor substrate having a P-type dopant region to support an N-channel transistor of the CMOS transistor structure and an N-type dopant region to support a P-channel transistor of the CMOS transistor structure, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure (Fig. 1)
- forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack (Ahmad, Fig. 2);
- forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (Ahmad, Fig. 3 –[126]);

Art Unit: 2823

forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (Ahmad, Fig. 3, Col. 1 line 66 to Col. 2 line 11 and/or Col. 2 lines 44-61);

forming at least one sidewall layer coupled to the layer of insulating material (Ahmad, Fig. 4 –[136]);

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks (Ahmad, Fig. 4);

forming a capping layer of contiguous silicon nitride over the semiconductor substrate (Ahmad, Fig. 5 - [138]).

Annealing is implicitly understood step that is required in order activate the dopants.

Ahmad is however silent upon explicitly annealing, after the formation of the capping layer and with the capping layer in place, then removing all of the capping layer after the annealing.

This sequence of steps was however conventionally known to one of ordinary skill in the art at the time of the invention.

At the time of the invention it was known in that the induced strain/stress in the channel region of a CMOS device can be modified by performing the annealing step with the capping layer in place. This known processing sequence when forming a CMOS device is disclosed by Chen et al. Chen discloses the sequence of steps comprising:

forming a capping layer of contiguous silicon nitride over the semiconductor substrate (Chen, Fig. 3 - [24]);

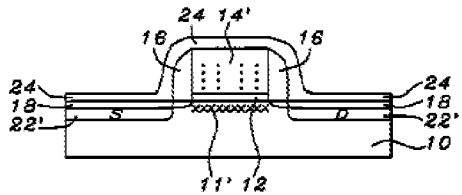


FIG. 3

annealing, after the formation of the capping layer and with the capping layer in place, the extension regions and the source and drain regions (Chen, Fig. 4 - [27] paragraph [0051]); and

and then teaches that the capping layer is capable of being removed after the annealing (Chen, Fig. 5 - [27] paragraph [0059]);

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Ahmad and Chen to enable the CMOS production step of Chen to be performed according to the teachings of Chen because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed CMOS production step of Chen and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

wherein said interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent (Ahmad, Col. 4 lines 8-15).

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the nitrogen concentration through routine experimentation and optimization to

Art Unit: 2823

obtain optimal or desired device performance because the nitrogen concentration is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

wherein the capping layer has a thickness in the range of 200-1000 angstroms (Chen, paragraph [0048], Ahmad discloses the capping layer however is silent upon the thickness).

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the thickness through routine experimentation and optimization to obtain optimal or desired device performance because the thickness is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

wherein the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds (Chen, paragraph [0051] RTA will be below 10 seconds).

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the

Art Unit: 2823

temperature through routine experimentation and optimization to obtain optimal or desired device performance because the temperature is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

Ahmad is silent upon the desired dopant concentration for the source and drain regions. It would however be obvious to one of ordinary skill in the art to be capable of selecting the proper doping concentration from conventionally known ranges to meet the desired design/operating parameters of the device being manufactured. For a supporting example of one of ordinary skill in the art disclosing the claimed convention doping concentration range see Wieczorek, paragraph [0034]. Wieczorek disclosed wherein the extension, source, and drain regions for the PMOS transistors have a dopant concentration in the range of about $1-2 \times 10^{20}$ atoms/cm³.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the dopant concentration through routine experimentation and optimization to obtain optimal or desired device performance because the dopant concentration is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the

Art Unit: 2823

optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

Regarding claims 19 and 20, the prior art references Wieczorek and Chen are silent upon the step of breaking vacuum during the processing, therefore the Examiner take the position the prior art does not teach “breaking vacuum” thus the process is understood to be performed without breaking vacuum.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARRETT J. STARK whose telephone number is (571)272-6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2823

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew S. Smith/
Supervisory Patent Examiner, Art
Unit 2823

12/5/2008
/J. J. S./
Examiner, Art Unit 2823